HP 3000 SERIES II
COMPUTER SYSTEM
MANUAL OF STAND-ALONE DIAGNOSTICS

STAND-ALONE
HP 30003A CPU DIAGNOSTIC

Diagnostic No. D420

HEWLETT PACKARD

30003-90001
Printed in U.S.A.

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1.0 INTRODUCTION

This diagnostic is divided into 14 sections, each of which is a separate program. The purpose of these tests is to performa checkon the HP 3000 Series II Computer System CPU. These test are able to indicate the problem at the instruction level.

1.1 These tests do not exhaustively check the memory. Memory can be checked using:

A. Memory Pattern Test, or
B. ROM Memory Test

1.2 This diagnostic will test anything that can be tried in the CPU by a Stand Alone Program. This includes all of the instructions and most of the conditions which result in interrupts and traps.

1.3 All control and reporting is implemented thru the HP 30354A maintenance panel.

1.4 The switch register or the internal switch register (ISR) controls the diagnostic. All reporting is done by coded halts. The Section Select Register in this diagnostic is used to select optional tests and contains special configuration data.

1.5 It is the responsibility of the user to check out the manual functions of the maintenance panel.

1.6 These tests will run on a CPU configurated CPU1. The CPU configuration %4 = CPU1.

1.7 This diagnostic has an automatic looping feature. Each step loops at least 1000 times before executing the next step. This feature can be defeated by setting bit 3 of the Section Select Register.

2.0 MINI-OPERATING INSTRUCTION

For use with a configured tape; if tape is not configured, refer to Detailed Operating Instructions, 4.0.

2.1 Section I

Load and run - CIR = Pause (%030020)

Press Run/Halt - Should Halt

Press Run/Halt - Should Run
Halt %15 indicates END of pass.

2.2 Section II through V

Load and Run.

Halt %15 indicates END of Pass.

2.3 Section VI through XIV

Load and Run - System Halt should occur.

Section #	CIR	SP2	SPI (Memory Data)
6	-	%120001	< > Ø
7	-	%120001	< > Ø
8	-	% 1	-
9	-	%117401	< > Ø
10	IXIT	%000000	-
11	PSEB	% 3	-
12	-	%120001	Ø
13	-	%117401	Ø
14	-	% 6	Ø

3.0 HARDWARE REQUIREMENTS

3.1 This diagnostic will run on a HP system with the minimum hardware needed to support .

3.2 The following are also required:

A. Maintenance panel . (Diagnostic can be run using the Control Panel, but only as a GO-NOGO check).

B. Listing of the microcode.

C. Listing of this diagnostic (including PMAP).

3.3 An SIO MUX and a Selector Channel Test Board or Mag Tape Controller are required for Sections III, IV, V.

4.0 DETAILED OPERATING INSTRUCTIONS

4.1 Connect the HP 30354A Maintenance Panel to the system and set the following Panel Switches.

SWITCH	POSITION
ERROR	INHIBIT
TIMERS	ENABLE
INTERRUPT	ENABLE

4.2 General Operating Procedures

Loading

The Diagnostic Tape is prepared by the HP Stand-alone Diagnostic Utility Program. The 14 sections are on the magnetic tape in cold load format (SDUP).

The procedure on Cold-loading diagnostics is:

Switch Register = %3006
Press ENABLE and LOAD
Press Run
Execution begins

4.3 Sections I through V

A. Perform Procedure stated in 4.2

B. Select Program options from Table I and press Run.

Note: If preconfiguration is used just press RUN. Diagnostic will begin execution.

4.4 Section VI through XIV.

A. Perform Procedure stated in 4.2

B. Push RUN.

Diagnostic will execute and the result should be a system halt (Refer to Table II).

Sections VI through XIV are the System Halt Tests and have no options.

4.5 Section I Instructions

The order in which the following steps are performed may vary. (Refer to 5.6 and following paragraphs.)

4.5.1 Diagnostic will begin execution with a Pause Instruction (CIR = 030020).

Press the RUN/HALT Switch and computer should halt.

Press the RUN/HALT Switch and the diagnostic will continue.

4.5.2 If the SR Register Test Option is selected (Section Select Register bit 2) then a Halt %6 occurs.

Check that CNTR (on the maintenance panel) = Ø.

Press RUN.

A Halt %6 should occur.
Check that CNTR = Ø.
Press RUN.
A Halt %7 should occur.
Check that CNTR = 2.
Press RUN.
A Halt %10 should occur.
Check that CNTR = 4.
Press RUN.
Diagnostic should continue.

4.5.3 If PB and PL Test is selected (Section Select Register bit 1)

A Halt %11 will occur. Check PB = %10004
P = %10017
PL = %10023

Press RUN to continue.

4.5.4 If the Switch Register test is selected (SSR bit 0) then a Halt %3 occurs.

Set all even switches on the control panel (%125252).

Press RUN.

A Halt %4 should occur.

Set odd switches on the control panel (%052525) and press RUN.

A Halt %5 should occur.

Restore the Switch Register options and press RUN to continue.

4.5.5 If bits Ø and 1 of the Switch Register are set the diagnostic will Halt %16 at the end of step to reconfigure.

Set the switch register for the Section Select Register options and press RUN.

A Halt %17 will occur to allow you to restore the Switch Register options.

Press RUN to continue.

4.6 Section II Instructions

There are no special options for Section II.

4.7 Section III Instructions

4.7.1 The diagnostic will run without any options selected.

The following assumptions are made:

1. System has a Mag. Tape in DRT 6
2. System has a Clock in DRT 3
3. System has a SIO MUX DRT = 127
4. System has a Selector Channel Maintenance Board 101 (optional See paragraph 4.7.6)

4.7.2 If Switch Register bit Ø and 1 are set diagnostic will halt at the end of step for the user to modify the SSR (Section Select Register). Refer to 4.5.4.

4.7.3 If SSR bit Ø is set computer will Halt %3 to allow the user to change the mag. tape DRT.
Enter new DRT number into the switch register and press RUN.
Computer should Halt %4 to allow user to restore switch register.
Press RUN to continue.

4.7.4 If SSR bit 1 is set computer will Halt %5 to allow the user to change the DRT of the clock.
Enter DRT into the switch register and press RUN.
Computer should Halt %6 to allow user to restore switch register options.
Press RUN to continue.

4.7.5 If SSR bit 2 is set the diagnostic will use the clock to test direct I/O instructions.

4.7 Section III Instructions (continued)

4.7.6 If SSR bit 4 is set the diagnostic will use the Selector Channel Test Board to test I/O instructions.

Note: An SIO MUX and a Mag Tape Controller or Selector Channel Test Board are required for this section.

4.7.7 If SSR bit 5 is set the diagnostic will Halt %7 to allow user to change the DRT of the Selector Channel Test Board.
Enter DRT into switch register and press RUN.
A Halt %10 should occur to allow the user to restore the switch register options.
Press RUN to continue.

4.8 Section IV Instructions

For SSR bits Ø, 1, 2, 4, 5, see section 4.7.

4.8.1 SSR bits 7-11 contain the memory size.
bits 7-9 contain amount of memory.
bits 10-11 contain upper bank numbers.

Memory Size	bits 7 8 9	Upper Bank	bits 10 11
64K	0 0 0	0	0 0
80K	0 0 1	1	0 1
96K	0 1 0	1	0 1
128K	0 1 1	1	0 1
160K	1 0 0	2	1 0
192K	1 0 1	2	1 0
224K	1 1 0	3	1 1
256K	1 1 1	3	1 1

4.8.2 If SSR bit 12 is set then diagnostic will Pause %12 for the Power Fail/Restart Test.
Turn power to computer off and then on using the SYSTEM DC POWER switch.
Computer should come up and continue running diagnostic.

4.9 Section V Instructions

See section 4.3.

5.0 OVERALL ORGANIZATION

The CPU diagnostic is divided into 14 sections, each of which is a cold-loadable separate program.

5.0.1 Section I includes about half of the instruction set. These instructions are the simpler ones and once tested are used to test other instructions.

5.0.2 Section II includes the rest of the instruction set except for the I/O instructions and the interrupt system.

5.0.3 Section III tests the I/O instructions.

5.0.4 Section IV tests the interrupt system.

5.0.5 Section V tests the bounds checking capability.

5.0.6 Sections VI through XIV are the system halt tests.

5.1 Instruction Set Testing

The following applies to Section I and II.
In Section I, the instructions are tested in an order which appears random. In Section II the instructions are tested in groups. The objectives in testing the instruction set are:

1. Check each possible line of microcode.
2. Include enough addressing modes so that each possible look-up table address is checked.
3. For instructions requiring a possible preadjust, test the instruction with different values of SR such that the preadjust will and will not be required.
4. Include enough cases to cover the operand and addressing fields of the instructions.

5.1.1 Where possible, all instructions are tested using instructions previously checked out. Exceptions are in testing the overflow, carry and index register. In these cases, instructions are tested in combination.

5.1 Instruction Set Testing (continued)

5.1.2 Not tested in sections I and II are conditions which result in and expected interrupt, system trap, or system halt. These conditions are tested in the later sections of the diagnostic.

5.1.3 Where possible, common paths in the microcode are not tested if they are used by a previous instruction.

5.1.4 All 24 possible addressing modes for the load instruction are tested. The minimum addressing modes required to test the pre-adder function for the remaining memory reference instructions include:
TBA P+D; TBA P-D;
STOR DB+D,I,X; STOR Q+D,I,X; STOR S-D,I,X; DB+D,I,X;
INCM Q+D,I,X; INCM Q=D,I,X: INCM S-D,I,X; LDB & STB with indexing (both direct and indirect)
STD & STB with indexing (both direct and indirect)
All 8 conditions both ways of the BCC P+ instruction.
The above are tested along with any other cases required to test each line of the microcode.

5.1.5 The SUBS,PSHR 0, AND SETR 0 instructions are used to initialize SR. Each following load instructions adds one to SR (maximum of 4) a SUBS or PSHR 0 instruction should result in SR=0; a SETR 0 instruction in SR=4.

5.1.6 No attempt is made to test all 4096 combinations of the stack opcodes. Each is tested in the A position with a NOP in the B position. In addition, some are tested in the B position with a NOP in the A position.

Also included randomly throughout the code is a previously tested stackop under test in the other. Included in the B positions are stackops %25, %52, and %77.

5.2 Listing

The diagnostic is coded in SPL . Sections I and II are mostly assemble statements while the later sections are mostly higher level statements. Generally, the comments toward the left side of the listing are program comments while those towards the right are error comments.

Included with the listing is the code option which gives the emitted code after each procedure or out block. Following each section is a PMAP which gives the procedure organization and linkage.

5.3 Error Analysis

1. Halt 1's are unexpected internal interrupts. CIR = %030361.
2. Halt 2's are unexpected external interrupts. CIR = %030362.
3. Halt %12's are error Halts. CIR = %030372.
4. Halt %13's are Halted at Step #. CIR %030373 (DB+5 contains current Step #)
   (XReg contains current Step #)
5. Halt %15 is halted after complete cycle. CIR = %030375.
6. Halt %16 - Halt to modify selection select register. CIR = %300376
7. Halt %17 - Halt to restore switch register. CIR = %300377
8. A BR* is used to indicate errors in user mode. CIR = %140000.

NOTE: CIR is the Current Instruction Register. If error is detected, the program should not be continued. Unexpected interrupts are irrecoverable. If an unexpected interrupt occurs, the address in the code when it occured can be determined from the stack marker and the CST table.

5.4 Memory Image After Cold Loading

Octal Location	
0	CSTP = %1340
1-3	0
4	0
5	Q11 = %7100
6	Z11 = %7776
7	0
10	0
11	Q12 = %7100
12	Z12 = %7776
14-777	DRT TABLE
1340-1357	CST TABLE

5.5 Preconfiguration

This diagnostic may be preconfigured using SDUP. This is done by modifying the DB Locations which contain configuration data.

DB	Definition
Ø	Internal Switch Register (ISR)
1	Section Select Register (SSR)

Sections VI through XIV do not have any options.

In Section I through V the ISR is preset to ØØØØØ1 if pre-configuration does not modify it.

The Section Select Register is preset to the following:

1. Section I = Ø
2. Section II = Ø
3. Section III = %020000
4. Section IV = %020000
5. Section V = %020000

Useful DB Locations

DB+2 Version and update level
DB+3 Section #
DB+5 Step #

Table I

Program Option for Sections I through V

INTERNAL SWITCH REGISTER (ISR)

Switch	Result
0	Select External Switch Register
1	Modify Section Select Register.
11	Loop on last step.
13	Halt at end of step.
15	Halt at end of complete pass.

Note: The ISR is preset to %000001 in all sections.

Section Select Register Options

1 SECTION I

BIT OR SWITCH	RESULT
0	Select Switch Register Test. (Halt 3,4 & 5.)
1	Select PB & PL Register Test. (Halt 11.)
2	Select SR Register Test. (Halt 6,7,8 & 10.)
3	Defeat looping option.

2 SECTION II

BIT OR SWITCH	
3	Defeat looping option.

3 SECTION III

BIT OR SWITCH	RESULT
0	Change Mag Tape DRT. (Halt 3 & 4.)
1	Change Clock-TTY DRT. (Halt 5 & 6).
2	Use Clock-TTY to Test I/O Instructions.
3	Defeat looping option.
4	Use Dummy Controller to Test I/O Instructions.
5	Change Dummy Controller DRT. (Halt 7 & 10.)

4 SECTION IV

BIT OR SWITCH	RESULT
0	Change Mag Tape DRT.
1	Change Clock-TTY DRT.
2	Use Clock-TTY for Interruptable Instructions.
3	Defeat looping option.
4	Use Dummy Controller for I/O Instruction.
5	Change Dummy Controller DRT.
7	Memory Size 000 = 64K
8	001 = 80K
9	010 = 96K
	011 = 128K
	100 = 160K
	101 = 192K
	110 = 224K
	111 = 256K
10	
11	

Section Select Register Options

4 SECTION IV (Cont.)

Upper Bank # 00 = 0
01 = 1
10 = 2
11 = 3

12	Power Fail Test.

5 SECTION V

BIT OR SWITCH	RESULT
3	Defeat looping option.

6 SECTION VI THROUGH XIII

These are the System Halt Tests and have no options.

5.6 SECTION I

5.6.1 Detailed Description of Tests

STEP #	DESCRIPTION
0	Outer block preliminary instruction tests. The following preliminary tests are done in the outer block: a. Load and Compare instructions. b. Some Conditional Branches. c. SR control tests. d. Repeat A&B as a function of SR. e. Stack-Ops f. Conditional Branches. g. Immediate instructions. h. Simple cases of the Memory Reference instructions.
1	PCAL to user segment. PL, PB Register check (optional).
2	Switch Register Test (optional)
3	More Stack-Op instruction tests.
4	Load Instruction-All addressing modes.
5	More Memory Reference instructions.
6	PSHR and SETR Instruction Tests.
7	Branch-All Addressing Modes.
10	Additional Tests - PLDA & PSTA.
11	LDB and STB Tests.
12	LDD and STD Tests.
13	Indirect Branch Tests.
14	Test BTST - 256 Combinations.
15	LDI and LDNI Tests.
16	LDPP and LDPN Tests.
17	Load and STOR Tests.
20	More Branch Tests.
21	Branch Condition Code Tests.
22	DABZ Tests.
23	CPRB Tests.
24	Exchange DB Tests.
25	NOP Test.
26	Non-privileged mode tests. a. LOAD DB+ and CMPI. b. INCA. c. BOV P+ d. SETR(X). e. EXIT. f. PCAL

5.6.1 Detailed Description of Tests (continued)

STEP #	DESCRIPTION
27	PCAL Test - User mode to User mode.
30	LSEA & SSEA Instruction Tests (Bank Ø only)
31	LDEA & SDEA Instruction Tests (Bank Ø only)
32	PCN Instruction Tests.

5.6.2 Instruction Test Order

I. String of tests in outer block Step Ø

A. Load & Compare Instructions

1. LDI
2. LOAD DB+
3. LDNI
4. CMPI
5. CMPN
6. CMP

B. Some Conditional Branches

1. BRE P+
2. BRO P+
3. BCC P+ (8 conditions-both ways)

C. SR Control

1. SUBS
2. PSHR Ø
3. SETR Ø
4. SR register check option

D. Previous tested instructions as a function of SR

1. SUBS
2. BRO
3. BRE
4. LDI & CMPI
5. LOAD & CMPM
6. LDNI & CMPN

E. Stackops, Conditional Branches, Immediate, and simple cases of Memory Reference Instructions

1. ZERO
2. DZRO
3. ZROB
4. INCA & BOV P+
5. INCA & BNOV P+
6. INCA & BCY P+
7. INCA & BNCY P+
8. DEL
9. DDEL
10. DELB
11. DUP
12. DDUP
13. DCMP
14. ADDS
15. DECA
16. INCB
17. DECB
18. IZBZ P+
19. DABZ P+
20. OR
21. XOR
22. AND
23. ORI
24. XORI
25. ANDI
26. ADD
27. ADDI
28. SUB
29. SUBI
30. MPY
31. MPYI
32. DIVI
33. DIV
34. LDXI & LDXA
35. LDXN
36. ACXI
37. SBXI
38. XAX
39. XBX
40. ZROX
41. LDXB
42. STAX
43. STBX
44. INCX
45. DECX

5.6.2 Instruction Test Order (continued)

46. ADAX
47. ADBX
48. ADXA
49. ADXB
50. IXBZ P+
51. DXBZ P+
52. LDPP
53. LDPN
54. LDX DB+
55. PSTA & PLDA
56. STOR DB+
57. LRA DB+
58. LRA P+
59. LRA P-
60. PSHR (S,Q, STATUS) & LRA S-
61. SETR (S,Q)
62. SXIT
63. SCAL
64. PCAL
65. EXIT
66. EXF

5.7 SECTION II

5.7.1 Detailed Description of Steps

STEP #	DESCRIPTION
0	Outer Block.
1	Field Instructions.
2	Bit Test Instructions.
3	Double Integer Instructions.
4	Loop Control Branch Tests.
5	Single Word Shifts.
6	Double Word Shifts.
7	Triple Word Shifts.
10	Four Word Shifts.
11	Floating Point Tests.
12	Move Tests.
13	MVB Tests.
14	MVBW Tests.
15	SCW Tests.
16	SCU Tests.
17	CMPB Tests.
20	List Search Tests.
21	Load Label Tests.
22	Privilege Mode Move Tests.
23	XEO Tests.
24	User Mode Tests.
25	TBX Tests.
26	Move to Data Segment Tests.
27	Move From Data Segment Tests.
30	Move Using Data Segment Tests.
31	Move Using Absolute Address Tests.
32	Load and Store Into System Table Tests.
33	Read and Set Process Clock Tests.
34	More Move Tests.

5.8 SECTION III

5.8.1 Detailed Description of Steps

STEP#	DESCRIPTION
0	Outer Block.
1	SED Instruction Tests. All Microcode paths of the SED Instruction are tested.
2	SMSK and RMSK Instruction Tests. The SMSK and RMSK Instructions are tested in combination.
3	Direct I/O Instruction Tests. The system clock is used to test the CIO, TIO, WIO and RIO instruction: CIO and TIO are tested in combination by writing, then reading the counting rate selector (CRS). WIO and RIO are tested in combination by writing, then reading the limit register (LR).
4	SIO Instruction Tests. The SIO Instruction is tested without interrupt by executing a two order SIO Program (SENSE, END). The device used is the Mag Tape.
5	Device Busy Tests. The following instructions are tested to see if the device is busy: SIO, RIO, WIO This is done by testing CC = CCG after the second of two consecutive I/O instruction, the first of which is an SIO instruction. The device used is the Mag Tape.
6	Clock Busy Tests. This step checks that an SIO call to the System Clock sets CC = CCG for Device Busy.
7	Non-Responding Device Tests. The following instructions are tested by addressing a non-existing device and checking CC = CCL non-responding device: SIO, RIO, WIO, CIO, TIO, SIN.

5.9 SECTION IV

5.9.1 Detailed Description of Steps

STEP #	DESCRIPTION
0	Outer Block.
1	More Exit Instruction Tests. This step checks the Exit Instruction when SM<Q. No interrupt is expected. Checked following the Exit Instruction is S. a. SR=0 S=SM=Q-1 b. SR=4 S=Q SM=Q-4
2	Status Overflow Tests. Integer Overflow is tested by setting status with %167403. Checked in segment one, STT #25 are parameter =1, status, X, Q, S, DB, DL, Z, and the contents of the 4 word marker.
3	User Trap Tests. For the following, the parameter, status, Q-1, and Q-2 is checked in segment 1, STT #25. a. Integer Overflow (addition of 2 registers) Parameter=1 b. Floating Point Overflow Parameter=2 c. Floating Point Underflow Parameter=3 d. Integer devide by 0 Parameter=4 e. Floating point divide by 0.0 Parameter=5
4	Unimplemented Instruction Tests For the following unimplemented instructions, STT #16, Segment 1 are checked. a. Instruction = %7200, Privileged Mode, Traps Enabled, SR=0 b. Instruction = %72, Privileged Mode, Traps Disabled, SR=0 c. Instruction = %72, User Mode, Traps Disabled, SR=0 d. Instruction = %20407 e. Instruction = %03600 f. Instruction = %2-357 g. Instruction = %20420

STEP #	DESCRIPTION
5	Privilege Instruction Tests. For the following exit tests, checked in Segment 1, STT# 22, Q-2. a. User to privilege exit (no swapping) b. User to user exit with bit 1 of Q-1 Bit 1 = Status (1) c. User to privilege exit to segment 4 with M bit set in CST entry for Segment 4. Also checked in segment 1, STT #22 are Q-1, and Q-6.
6	Privileged Mode Instruction Tests. For the following instructions in user mode, checked in segment 1, STT#22 are Q-2. LLSH PAUS SETR XCHD MVBL SED TIO SMSK HALT MABS MTDS MFDS LOCK UNLK IXIT DISP PSDB PSEB SIO WIO RIO CIO SIN CMD PSHR SETR PLDS LSEA LDEA PSTA SSEA SDEA PCN LST SST MVLB

5.9.1 Detailed Description of Steps (continued)

STEP #	DESCRIPTION
7	Trace Bit Tests. PCAL to segment, whose trace bit is set checked in Segment 1, STT# 32, are parameter, S, Q-1, Q-2, Q-5, and Q-6. Exit Ø with Q-2 negative. Checked in Segment 1, STT #33 are parameter, S, Q-1, Q-2.
10	STT Uncallable Tests. PCAL to Segment 4 from Segment 3 in user mode. Uncallable bit set in Segment 4 CST STT Entry. Checked in Segment 1, STT# 33 are parameter, S, Q-1, Q-2.
11	Absent Segment Tests. PCAL to absent segment, checked in Segment 1, STT# 31 are S, Q-1, parameter, Q-2, Q-5, Q-6. Exit 0 to absent segment, checked in Segment 1, STT#31, are parameter S, Q-1, Q-2.
12	Stack Underflow Tests. Checked in Segment 1, STT# 21, S, Q-2. a. Exit instruction in user Mode such that new S<DB. b. Exit instruction in user mode such that new Q<DB.
13	CST Violation Tests. Checked in Segment 1, STT# 18, are S, and Q-2. a. PCAL to Segment Ø. b. Exit to Segment Ø while not on the ICS. c. PCAL to Segment where CSTL<2*SEGMENT#.
14	STT Violation Tests. SCAL 0 with external label in TOS. Checked in Segment 1, STT#17, are S, Q-2.
15	Illegal Address Tests. Indirect branch to an address outside the Code Segment. Checked in Segment 1, STT #1, are S, Q-2.
16	Module Violation Tests. PLDA Instruction with X=Address of a non-exisiting core location. Checked in Segment 1, STT#2, are S, and Q-2.
17	Module Interrupt Tests. Checked in Segment 1, STT# 7, are Parameters, S, Q, (Q1-5) -3.

STEP #	DESCRIPTION
	The following tests use the CMD instruction: a. RWA to memory module with SR>=2. b. RNWA to memory module with SR=0. 1. Check that interrupt doesn't occur until interrupts are enabled. 2. Check that interrupt occurs when interrupt is enabled. 3. Check that the contents of the tested memory location is %177777. c. RWA to CPU module. d. Check that if on the dispatcher and status (1)=0 that a module interrupt is held off.
20	Power Fail Tests. Optional-checked are the ability to save QI-5 when power fails, and the ability to restore QI-5 when power is restored, and to continue.
21	SIN Instruction Tests. Check External Interrupt following a SIN Instruction. Checked in the interrupt routine are parameter, status, S, Q, Z, DB, DL, QI-5, the contents of the 4 word marker on the user stack, and the pushed DB on the user stack. Check that interrupt occurs if status (1) = 1, and mask = -1. Check that mask register = 0 holds off external interrupts.
22	SIO External Interrupt Tests. Checked in the interrupt routine are parameter, status, Q, Z, DB, S, QI-5, and the pushed DB on the user stack. This SIO program is a 2-order call sense, interrupt, with end. Checked on return are the DRT pointer, and the status word in the SIO program. The status word was %177777. Check to see that at least one bit is 0, QI-5, (QI-5)-3, S, parameter, and DB.
23	Interruptable Instruction Tests. The ability to interrupt the following instruction is tested. a. PAUS b. MOVE c. MVB d. MVBL e. LLSH

5.9.1 Detailed Description of Steps (continued)

STEP #	DESCRIPTION
24	Interrupt Between Two Stack-Ops Test. Check that an interrupt can occur between 2 stack-ops. The test is implemented by doing an assemble (add,add); with traps enabled and with operands such that the first add will cause an integer overflow. Checked in Segment 1, STT#25, are parameter=1, status, Q-1, Q-2, and the sum in Q-4. Also checked on return are the sum and the reference bit.
25	Exit to Segment 0 Interrupt Test. Exit back to an Interrupted Segment Ø. Checked in Segment 1, STT#25, following an integer overflow are S, and parameter. Checked in Segment Ø on return is the parameter on the TOS.
26	Simultaneous Trap and Interrupt Test. Check results of simultaneous interrupts consisting of an overflow trap and an external interrupt. Expected overflow marker to be laid down first, followed by external interrupt marker.
27	Multiple Stack Overflow Tests. Check that stack overflows while on the ICS do not result in QI-5 being changed. a. Dispatcher Flag = Ø. b. Dispatcher Flag - 1.
30	IXIT. a. Return to interrupted process. b. Same as 'a' but a DISP had been executed while pseudo-disabled. c. Return to interrupted interrupt routine. d. Start dispatcher instead of returning to interrupted process. e. Return to interrupted dispatcher. f. Same as 'e' except a DISP instruction had been executed while pseudo-disabled. g. Restart dispatcher instead of returning to interrupted dispatcher. h. Dispatcher IXIT to new process.

5.9.1 Detailed Description of Steps (continued)

STEP #	DESCRIPTION
31	Special Bank Test using special E.T.
32	Data Segment Table Violation, Trap Tests.
33	LSEA & SSEA Tests. (Executed if Second Bank available).
34	LDEA and SDEA Tests. (Executed if Second Bank available).
35	MTDS and MFDS Instruction Tests.
36	MDS Instruction Tests.
37	MABS Tests (Executed if Second Bank available).
40	More I/O Tests. The following SIO orders are tested: 1. Return residue 2. Write 3. Sense 4. Read 5. Conditional Jump 6. Unconditional Jump
41	Bank SIO: This test will run SIO programs with data in banks other than Ø.
42	This step tests the Double Integer Multiply (DMUL) and Double Integer Divide (DDIV)

5.10 SECTION V

5.10.1 Detailed Description of Steps

STEP #	
0	Outerblock The outer block controls the operation of the diagnostic. It tests the switch register for program and configuration options and executes them.

5.10.1 Detailed Description of Steps (continued)

STEP #	DESCRIPTION
1	Additional Register Tests. Checked are all bits in the 5th stack registers plus the 8 least significant bits of the Status Register.
2	Unconditional Bounds Tests (UBNT) 18 cases are tried in Privileged Mode. Expected is an illegal address interrupt to Segment 1, STT #2. Checked in Delta P in Q-2.
3.	Unconditional Bounds Test (UBNT) 18 cases are tried in user mode. Expected is an illegal address interrupt to Segment 1, STT #2. Clocked is Delta P in Q-Z.
4.	Bounds Test. (BNDTP) 25 cases are tried in Privilege Mode no interrupts are expected.
5.	Bounds Test. (BNDTN) 25 cases are tried in user mode. Expected is on illegal address interrupt in Segment 1, STT #2. Checked is Delta P in Q-2.
6	Bounds Violation Tests (BNDVP). 3 cases are tried in Privilege Mode. No interrupts are expected.
7	Bounds Violation Tests (BNDVN) 3 cases are tried in user mode. Expected is an illegal address interrupt to Segment 1, STT #2.
10	Stack overflow Tests. (STOV) 3 cases are tried in Privileged Mode. Expected is an stack overflow interrupt to Segment 1, STT #20.
11	Stack underflow Tests (STUNP) 4 cases are tried in Privileged Mode. No interrupt is expected.
12	Stack underflow Test (STUNN) 4 cases are tried in user mode. Expected is an stack underflow interrupt to Segment 1, STT #21.
13	STT Violation Tests (STTV) 4 cases are tried in Privileged Mode. Expected is an interrupt to Segment 1, STT #17 (STT Violation).
14	STT uncallable - Privileged Mode (STTV). No interrupt is expected.

5.10.1 **Detailed Description of Steps** (continued)

STEP #	DESCRIPTION
15	Split Stack Byte Addressing Test (BATSS) The LDB, STB, and MVB instructions are tested in Privileged Mode with both DB and E (effective word address) not between DL and S. These tests include cases where both DB and E are S.
16	DL-DB area addressing Tests (DLDBT) The ability of the following instructions to address the DL-DB area are tested in user mode. a. LOAD b. LDD c. LDB d. STOR e. STD f. MOVE
17	Upper Half of 64K memory DL-DB area Addressing Tests. The ability to address the DL-DB area in the upper half of memory (32K) in Privileged Mode is tested using the MOVE, LDB, and MVB instructions.

5.11 SECTION VI - XIV

These sections contain the System Halt Tests. Each section has only one test per section.

Section	Description
VI	Interrupt to Segment 1 where absent bit is set in CST entry for Segment 1.
VII	Code Segment Table Length = Ø
VIII	Absent bit set = 1 in any referenced CST entry while executing on the ICS.
IX	(Q1-18) = 0 when executing a PSEB Instruction.
X	STT Length Violation or STT No. points to an external label which should be local, or LLBL encounters an illegal label in Segment 1.
XI	Stack overflow on the ICS.
XII	External Interrupts Enable Status (1)=Ø while executing a Lock Instruction.
XIII	Unable to reset interrupt line of interrupting device during on IXIT instruction.
XIV	A Lock Instruction is executed while the Interrupt System is off.

TABLE II. SYSTEM HALT CONDITIONS

Section #	CIR	SP2	SP1 (Memory Data)
6	-	120001	< > 0
7	-	120001	< > 0
8	-	1	-
9	-	117401	< > 0
10	IXIT	000000	-
11	PSEB	3	-
12	-	120001	0
13	-	117401	0
14	-	%6	-

6.0 INITIALIZATION FOLLOWING COLD LOAD

Absolute Memory Address (Octal)	Contents (Octal)	Code	Comments
1231	040014	Load CØ	<<TOS:=S-DB>>
2	040014	Load C1	<<TOS:=Q-DB>>
3	040014	Load C2	<<TOS:=Z-DB>>
4	040014	Load C3	<<TOS:=DL-DB>>
5	000600	Zero	<<TOS:=DB BANK>>
6	040013	Load C4	<<TOS:=DB>>
7	027563	SETR %163	<<Set DB,DBBANK,DL,Z,>> <<Q,S>>
40	040012	LOAD C5	<<Form Exit marker X=Ø>>
41	040012	LOAD C6	<<ΔP>>
42	040012	LOAD C7	<<STATUS>>
43	100012	LOAD C10	<<DQ>>
44	031400	EXIT Ø	<<Go to start of Diag.>>
45	007200	CØ CON %7200	<<S-DB>>
46	007204	C1 CON %7204	<<Q-DB>>
47	007660	C2 CON %7660	<<Z-DB>>
50	177770	C3 CON %-10	<<DL-DB>>
51	002000	C4 CON %2000	<<DB>>
52	000000	C5 CON %0	<<X>>
53	000000	C6 CON %0	<<ΔP>>
54	100003	C7 CON %100003	<<STATUS>>
55	000004	C10CON %4	<<ΔQ>>
56			